

2-12-03 03  
PATENT APPLICATION  
Q-61090

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yasunobu IWATA, et al.

Appln. No. (PCT/JP98/03402

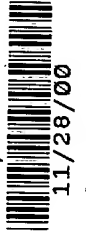
Group Art Unit:

Filed: November 28, 2000

Examiner:

For: LADDER CIRCUIT EDITING SYSTEM

JC841 U.S. PTO  
09/722306



**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR §§ 1.97 and 1.98**

Assistant Commissioner of Patents  
Washington, D.C. 20231

Sir:

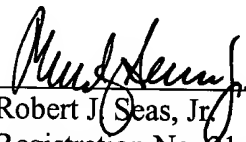
Pursuant to Applicants' duty of voluntary disclosure under Rule 56, and for the Examiner's convenience, we submit herewith:

- a) a form PTO-1449 listing four (4) references of potential relevancy; and,
- b) a complete copy of each reference.

No certification or fee is required.

Regarding the concise explanation of relevancy requirement for foreign language documents, an English-language abstract is attached for each reference.

Respectfully submitted,

  
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Registration No. 21,092

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Date: November 28, 2000